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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHAN JOURDAN, PER HAMMARLUND, AVINASH SODANI, JAMES ALLEN, FRANCIS MCKEEN, and PIERRE MICHAUD

Appeal 2008-005499
Application 10/676,310
Technology Center 2100

Before JOSEPH L. DIXON, LANCE LEONARD BARRY, JEAN R. HOMERE, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-22. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

The Appellants describe the invention at issue on appeal as follows:

> A method and system for multiple branch paths in a microprocessor is described. The method includes assigning an identification number (ID) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs, determining whether one or more branches are predicted correctly, determining which of the one or more branch paths are dependent on a mispredicted branch, and determining whether one or more of the plurality of uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs.

(Spec. 17.)

ILLUSTRATIVE CLAIM

1. A method comprising:

assigning an identification number (ID) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs;

determining whether one or more branches are predicted correctly;

determining which of the one or more branch paths are dependent on a mispredicted branch; and

> determining whether one or more of the plurality of uops belong to a branch path that is dependent on the mispredicted branch based on their assigned IDs.

REJECTIONS

Claims 1, 2, 6-13, and 17-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,065,115 ("Sharangpani").

Claims 3-5 and 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharangpani and U.S. Patent Application Publication No. 2003/0061258 ("Rodgers").

CLAIMS 1, 2, 6-13, AND 17-22

Based on the Appellants' arguments, we will decide the appeal of claims 1, 2, 6-13, and 17-22 based on claim 1 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii). The Examiner finds that "Sharangpani discloses a method comprising: assigning an identification number (ID) (Fig. 5 tag 504) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs." (Ans. 3.) The Appellants argue that "Sharangpani teaches a *single assignment to a group of instructions* rather than an assignment '*to each of a plurality of micro-operations (uops)* ' (emphasis added)." (Reply Br. 3.[2]) Therefore, the issue before us is whether the Examiner erred in finding that Sharangpani assigns an ID to each of a plurality of micro-operations as required by representative claim 1.

[2] The Appellants omit page numbers from the first four pages of their Reply Brief. In the future, however, we ask them to include page numbers on *all* pages of their reply briefs to facilitate identification.

FINDINGS OF FACT

Sharangpani discloses "[a] microprocessor for efficient processing of instructions in a program flow including a conditional program flow control instruction, such as a branch instruction." (Abstract, ll. 1-3.) More specifically, "[t]he processor 101 of the invention . . . includes stream management logic 109 for managing processing of one or more instruction streams concurrently in the instruction pipeline of the processor 101. The stream management logic 109 . . . includes branch processing and prediction logic 316 and stream control logic 314." (Col. 6, ll. 41-46.) For its part, "the stream control logic 314 includes one or more stream tables 330. The stream table 330 operates to keep track of the multiple instruction pointers used to control processing of multiple instruction streams in the processor pipeline." (Col. 9, ll. 34-38.)

ANALYSIS

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim, and that anticipation is a fact question . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.,* 730 F.2d 1452, 1457 (Fed. Cir. 1984)). Here, the Examiner relies on Sharangpani's tag 504 to disclose the claimed ID assigned to each of a plurality of micro-operations to identify a branch path to which each micro-operations belongs. For its part, the reference explains that the "stream table 330 . . . includes a field 504 for storing a tag which uniquely identifies the instruction stream associated with a particular instruction pointer." (Col. 10, ll. 6-8.) By assigning a tag to a stream of instructions, Sharangpani assigns the tag to each instruction in the stream.

The Appellants argue that "the cited claim language as a whole explicitly requires that a separate ID is assigned 'to *each* of a plurality of micro-operations (uops)' (emphasis added)." (Reply Br. 2.) "[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

Here, claim 1 does not require that the ID assigned to each micro-operation be "separate." i.e., unique. We refuse to read such a requirement into the representative claim. Assigning the same ID to each micro-operation in one of the reference's instruction streams is enough to anticipate the disputed limitations. Based on the aforementioned facts and analysis, therefore, we conclude that the Examiner did not err in finding that Sharangpani assigns an ID to each of a plurality of micro-operations as required by representative claim 1.

CLAIMS 3-5 AND 14-16

Based on the Appellants' arguments, we will decide the appeal of claims 3-5 and 14-16 based on claim 3 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii). The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of invention to have included Rodgers' sequence numbers "in Sharangpani's processor for the benefit of ensuring proper operation." (Ans. 8.) The Appellants argue that "Rodgers changes Sharangpani's principle of operation of assigning a tag to *a group of instructions* for retirement." (Reply Br. 5.) Therefore, the issue before us is

whether the Examiner erred in combining teachings of Sharangpani and Rodgers.

FINDINGS OF FACT

Rodgers includes the following explanation of multithreaded processor design:

> Multithreaded (MT) processor design has recently been considered as an increasingly attractive option for increasing the performance of processors. Multithreading within a processor, inter alia, provides the potential for more effective utilization of various processor resources, and particularly for more effective utilization of the execution logic within a processor. Specifically, by feeding multiple threads to the execution logic of a processor, clock cycles that would otherwise have been idle due to a stall or other delay in the processing of a particular thread may be utilized to service a further thread.

(¶ [0003].)

The same reference includes the following disclosure:

> A sequence number . . . is given to each microinstruction to track the logical order thereof within a thread as the microinstruction is processed . . . . The sequence number attributed to each microinstruction is stored together with status information for the microinstruction within a table 180 . . . within the reorder buffer 162.

(¶ 0064.) "Entries within the table 180 are, in accordance with the sequence numbers, allocated and de-allocated in a sequential and in-order manner." (¶ 0080.)

ANALYSIS

The presence or absence of a reason "to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)).

Here, Sharangpani discloses a processor for efficiently processing instructions as found regarding the first group of claims. For its part, Rodgers explains that multithreading within a processor provides for more effective utilization of the processor's resources. The latter reference assigns a sequence number to each microinstruction to track the logical order thereof within a thread as the microinstruction is processed. Entries within table 180 are, in accordance with the sequence numbers, allocated and de-allocated in a sequential and in-order manner.

We are persuaded that the advantages of multithreading disclosed by Rodgers would have given one skilled in the art reason to implement MT in Sharangpani's processor. To do so, the former reference explains that sequence numbers must be assigned to each microinstruction. Consequently, we agree with the Examiner that one skilled in the art would have had reason to assign sequence numbers to microinstructions in Sharangpani.

We are unpersuaded that such a use of sequence numbers would have required changing Sharangpani's assigning of a tag to a group of instructions for retirement. Based on the aforementioned facts and analysis, we conclude

that the Examiner did not err in combining teachings of Sharangpani and Rodgers.

DECISION

We affirm the rejections of claims 1-22.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(v).

AFFIRMED

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